Investigation of LC-Resonance Driving in Disconnector Bus-Transfer Testing

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SUMMARY
The ability to transfer load currents between parallel busbars is one of the main requirements for most disconnector switches in gas insulated as well as air insulated substations today. As such, the capability limits and testing methods are internationally standardized in IEC 62271-102. The test circuit dictated in this standard is the Thévenin equivalent of the high current, power frequency approximation of two parallel busbars supplied by an AC current source. This setup inevitably couples different factors influencing the bus-transfer switching process by directly specifying the pre-switching current through the disconnector switch and recovery voltage expected across it after successful switching.

To facilitate a more detailed and direct investigation of bus-transfer switching processes, a different test method is suggested and consequently implemented as a proof of concept. The suggested method entails the use of an AC current source to drive a current through two parallel impedances representing different sections of a busbar. The disconnector switch under test is placed in series with one of the impedances.

In order to analyze the feasibility of such a setup, a proof of concept current source along with two parallel impedances was built. The main design goal for the current source was to provide AC currents over a large range of magnitudes at a constant frequency. In addition, the current provided by the source must not be influenced by the bus-transfer switching process. To fulfill these requirements, an LC-resonance circuit with an adjustable resonance frequency and a substantial initial energy storage capacity was chosen. Its applicability was verified in numerous switching cases of different specifications.

The impedances representing substation busbars in the test setup were designed with a main focus on adjustability and precision. The resistance and inductance components were modelled after typical GIS substation values for lengths between 10 m and 600 m. Due to the conductor being comprised of overhead line cable, virtually any length in this range can be represented with minimal effort. Experimental verification has demonstrated that this type of test setup ensures direct comparability between laboratory tests and substation processes due to the ability to directly measure both parallel currents and the recovery voltage occurring at the disconnector after successful switching. This feature can prove beneficial for non-standard testing cases such as failure analysis and substation planning which require precise modelling of substation characteristics as well as sophisticated measurements.

KEYWORDS
Bus-transfer, Disconnector switch (DS), High-current, LC-oscillation, IEC, Non-standardized testing

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BACKGROUND

Large-scale investigations of switching phenomena in EHV and UHV substations by Cigré WG A3.28 [1] have recently reaffirmed the importance of bus-transfer switching by disconnector switches (DS) for all substation types (i.e. GIS, AIS and MTS). A large diversity of switching cases in terms of bus-transfer current as well as loop length and inductance per unit length was highlighted. Due to its nature as a high current power frequency switching case, bus-transfer can be modelled as a current commutation between two parallel paths as shown in Figure 1a [2]. The resistances $R_1$ and $R_2$ as well as the inductances $L_1$ and $L_2$ of both parallel current paths are usually approximated by the typical per unit length values $R'$ and $L'$ of a certain type of switchgear scaled by the length of the paths $d_1$ and $d_2$ as follows

$$Z_i = d_i(R_i' + j\omega L_i'), \quad i = \{1,2\}.$$  \hfill (1)

Typical values for $L'$ for 245 kV to 1100 kV substations can be found between 200…300 nH/m for GIS and between 0.8…1.4 μH/m for AIS, while $R'$ is commonly found between 5…10 μΩ/m. Thus, for many power frequency applications the approximation of the impedance of either path as their inductance is valid:

$$|Z_i| \approx \omega d_iL'_i.$$  \hfill (2)

In terms of path lengths, minimum values of 5.5 m and maximum values of 650 m were found in the survey [1].

The currents before switching ($t < t_s$) and during switching ($t_s \leq t \leq t_e$) for this model are given by

$$i_2(t) = i_{tot}(t) \cdot \frac{d_1}{d_1 + d_2} \text{ for } t < t_s$$  \hfill (3)

and

$$i_2(t) = i_{tot}(t) \cdot \frac{d_1}{d_1 + d_2} - \frac{u_{DS}}{R'(d_1 + d_2)} \cdot \left(1 - e^{-\frac{R't}{L'}}\right) \text{ for } t_s \leq t \leq t_e,$$  \hfill (4)

respectively, under the approximation of a constant switching arc voltage $u_{DS}$, which has been shown to be reasonable for slow-moving DS and short bus-transfer times [3]. After successful commutation of $i_2$ onto the parallel path ($t > t_e$), the recovery voltage $u_2^{rv}$ appears across the open DS.

$$u_2^{rv}(t) = Z_1 \cdot i_{tot}(t) \text{ for } t > t_e$$  \hfill (5)

$$\approx \omega d_1 L' \cdot i_{tot}(t)$$  \hfill (6)
IEC 62271-102 concerning bus-transfer switching mandates testing of DS according to the circuit shown in Figure 1b [4]. This circuit represents the Thévenin equivalent of Figure 1a with respect to the current source and path one. The following equations relate the properties between the two circuits:

\[ i_{BT} = i_2(t < t_e) \]  
\[ u_{BT} = i_{tot} \cdot Z_1 = u_2^{gy}(t > t_e) \]  
\[ Z_{BT} = Z_1 + Z_2. \]  

The capability limits of DS are specified by IEC 62271-102 (Annex B) according to the recovery voltage \( u_{BT} \) and the maximum bus-transfer current \( i_{BT} \). The first is given as an r.m.s. value specific to every voltage level for GIS and AIS while the latter is defined to be maximally 80% of the rated current or 1600 A, whichever is lower. A notable exception are 1100 kV and 1200 kV DS for which no absolute upper current limit exists. By solely specifying \( u_{BT} \) and \( i_{BT} \), however, the standard inevitably couples the various influences highlighted in equations (3) – (5). Namely the values of inductance and resistance per unit length which are technology and manufacturer specific become inseparable from the maximum commutation loop length \( d_1 + d_2 \) which in turn is determined by the configuration and construction of a given substation. Additionally, specifying the ratio of bus-transfer current and rated current to be 80% limits the ratio of \( d_1/(d_1 + d_2) \) to the same number except for cases which fix the maximum bus-transfer current of 1600 A regardless of the rated current.

**ALTERNATIVE TEST METHOD**

As an alternative to employing a high current voltage source as suggested by IEC 62271-102 in Figure 1b, the equivalent circuit from Figure 1a could also be used directly to investigate bus-transfer switching. This approach would allow decoupled adjustments of the total current \( i_{tot} \), the impedance ratio \( d_1/(d_1 + d_2) \) and total impedance \( Z_1 + Z_2 \), which would automatically establish \( u_2^{gy} \) across the open DS. A number of scenarios are conceivable which potentially benefit from this testing method. One of which is limit testing of new or improved prototype DS, which might require gradual adjustments of the path impedances while keeping a constant total current. Another scenario is non-standard DS testing for specific application cases outside of the established IEC standard, for example preliminary planning of individual substations and post-accident failure analyses. Furthermore, test cases for low frequency or direct current applications in which the approximation in equation (6) does not hold require an alternative method of testing due to impractically low recovery voltages.

In order to investigate the feasibility and viability of such a full bus-transfer test setup, a proof of concept implementation was built to achieve the following two main goals. Firstly, the resistances \( R_1 \) and \( R_2 \) as well as the inductances \( L_1 \) and \( L_2 \) of both parallel paths were to model typical values for GIS substations of varying lengths. Secondly, precise control over a significant range of the total current \( i_{tot} \) with minimal interaction between the bus-transfer process and its current source was desired.
IMPEDANCE DESIGN

For the voltage levels of 420 kV and 550 kV, the recent survey by Cigré WG A3.28 found all investigated GIS to feature inductances per unit length of 200 nH/m and resistances per unit length in the range of 5…10 μΩ/m. The shortest bus-transfer path length was found to be 5 m while the longest one was 500 m. Despite the dominance of the inductance in the power frequency recovery voltage given in equation (6), it is evident from equation (4) that both, inductance and resistance, of a bus-transfer loop influence the bus-transfer switching current. In terms of an equivalent impedance for laboratory tests, this leads to the necessity of a design exhibiting a linear increase of resistance with inductance. While evaluating impedance designs and shapes using tables from F. W. Grover [5], it was determined that a helical conductor assembly of small conductor radius, large outer radius and considerable pitch was needed in order to achieve the desired linear dependency of inductance and resistance. As conductor material, conventional overhead line cable was found to display multiple beneficial properties for this application. The uninsulated surface allows for precise tapping of the coil at arbitrary positions by means of high current specific clamps while keeping the conductor in one continuous piece to keep contact resistance to a minimum. Additionally, the cable itself offers favorable conductivity and excellent heat dissipation. The specific overhead line cable chosen for this application is a type 264-Al/34-ST1A conductor with a resistance per unit length of 109.4 μΩ/m at 20°C at a diameter of 22.4 mm. Figure 2a shows the range of different calculated inductance values which can be achieved for a coil featuring a major radius of 0.5 m and an axial pitch of 10 cm. From Figure 2b it is evident that these inductance values cover the required range of GIS bus lengths.

Figure 2a: Inductance (blue) and resistance (green for one wire, red for two parallel wires) per turn (n) of the helical coil.

Figure 2b: Equivalent length of a typical GIS in terms of different properties of the helical coil per turn.

However, the figure also indicates that for n < 9, the predicted resistance of this design (red) corresponds to a length of GIS bus greater than the length corresponding to the inductance. For this reason, a second cable was added in parallel, effectively halving the resistance (green). For applications requiring a precise ratio of resistance per inductance, additional trimm resistors can be added in series. In case very short sections of GIS bus in the range of a few meters are to be modelled, contact resistance of the taps renders the use of the coils impossible. Instead, a direct connection with high cross-section, low inductance stranded copper wire is made.
**LC OSCILLATING CURRENT SOURCE**

In addition to the current amplitude and frequency, the primary requirement for the current source employed in the bus-transfer setup was minimal interaction between the bus-transfer process and the current source. To this end, a series resonant circuit capable of storing significantly higher energies than dissipated by the switching process while assuring a source voltage larger than the anticipated switching arc voltage was designed. The source capacitance was provided by 120 parallel connected pulse capacitors of 7.7 μF \((C_s = 923 \text{ μF})\) and a maximum charging voltage \(U_{c0}\) of 15 kV. To achieve a resonant frequency \(f_s\) between 50…60 Hz two coupled air coils with a total inductance \(L_s\) of 9.2 mH were utilized. The total resistance \(R_S\) of the series connection of the capacitor banks and the inductor was measured to be 285 mΩ, resulting in an oscillation frequency of 54.5 Hz and a Q-factor of 11.1. The main contributors to this resistance are the aluminum windings of small cross sections of the main inductance. The aforementioned impedances and the GIS DS under test were placed on the current return path as presented in Figure 3. To initiate and subsequently interrupt the source current \(i_{tot}\), a medium voltage vacuum circuit breaker was used for its favorable insulation strength in open position and its low contact resistance in closed position. Due to the negligible magnitude of the impedances of the bus-transfer paths as compared to \(R_S\) and \(L_S\), the total current \(i_{tot}\) can be approximated by the analytical solution of the series oscillation of \(C_S\), \(L_S\) and \(R_S\), according to

\[
i_{tot}(t) \approx -\frac{U_{c0}}{\omega_S L_S} \cdot e^{-\frac{R_S}{2\omega_S L_S}t} \cdot \sin(\omega_S t) .
\]

(10)

It is evident from this equation, that the magnitude of the oscillating current can be adjusted by simply varying the initial capacitor voltage \(U_{c0}\). Taking into account the damping due to ohmic losses, the current source can deliver a maximum initial current peak of 4.5 kA.

To operate this current source, a number of auxiliary devices had to be interfaced as highlighted in Figure 3. Before any test, the capacitor bank is charged by an external charging unit which is subsequently isolated by a remote-controlled spark gap to avoid exposure to voltage reversal. The setup includes a second spark gap which automatically discharges the capacitors after only a few half-waves to prevent excessive oscillations and to dampen transient overvoltages when interrupting the main current by opening the vacuum circuit breaker. The operation of the circuit breaker, DS motor and auxiliary spark gaps is performed by an autonomous, central control system which guarantees a high repeatability of the individual experiment runs.

![Figure 3: Complete setup including control signals (blue) and measured variables (red).](image-url)
RESULTS AND DISCUSSION

To verify the operating principle of the LC oscillating current source, numerous bus-transfer switching scenarios with varying impedances and currents were conducted. Subsequently, two example tests using the same source settings but different impedance configurations are highlighted. Table 1 shows the impedances used for the two parallel paths of both examples, where $n_1$ and $n_2$ denote the number of turns of the aforementioned coils which were used in paths one and two. From the resulting inductances ($L_1$ and $L_2$) and resistances ($R_1$ and $R_2$) the power factors $\text{pf}_1$ and $\text{pf}_2$ were calculated as $\frac{R_i}{\sqrt{((\omega L_i)^2 + R_i^2)}}$. The equivalent lengths of GIS $d_1$ and $d_2$ were calculated using an inductance per unit length of 200 nH/m.

![Figure 4a: Two initial periods of example a).](image)

![Figure 4b: Two initial periods of example b).](image)

![Figure 4c: Bus-transfer process of example a).](image)

![Figure 4d: Bus-transfer process of example b).](image)

**Table 1:** Impedance configurations of examples a) and b).

<table>
<thead>
<tr>
<th></th>
<th>$L_1$ [μH]</th>
<th>$R_1$ [μΩ]</th>
<th>$n_1$ [turns]</th>
<th>$\text{pf}_1$ [%]</th>
<th>$d_1$ [m]</th>
<th>$L_2$ [μH]</th>
<th>$R_2$ [μΩ]</th>
<th>$n_2$ [turns]</th>
<th>$\text{pf}_2$ [%]</th>
<th>$d_2$ [m]</th>
</tr>
</thead>
<tbody>
<tr>
<td>a)</td>
<td>22</td>
<td>1000</td>
<td>1.5</td>
<td>13</td>
<td>100</td>
<td>3</td>
<td>550</td>
<td>0</td>
<td>47</td>
<td>15</td>
</tr>
<tr>
<td>b)</td>
<td>110</td>
<td>3920</td>
<td>12.5</td>
<td>10</td>
<td>550</td>
<td>20</td>
<td>760</td>
<td>4.5</td>
<td>11</td>
<td>100</td>
</tr>
</tbody>
</table>

Example a) models a bus-transfer scenario with a short, high ohmic section of GIS bus containing the DS and a longer parallel path with a power factor typical for GIS. Example b) represents longer sections of GIS bus featuring a parallel path of 550 m and a path of 100 m in series to the DS. For both tests, a maximum total current $i_{\text{tot}}$ of 1.5 kA was desired, which according to equation (10) necessitated an initial capacitor voltage $U_C^0$ of 5 kV. Due to the similar impedance ratios between the two parallel paths in both examples, a similar distribution of currents before switching was expected as by equation (3).

Figures 4a - d show one measurement for each of the aforementioned examples, key parameters of these measurements are summarized in Table 2. The plotted signals correspond to the sensors shown...
in Figure 3 except for \( i_2(t) \) which is calculated as the difference of \( i_{tot}(t) \) and \( i_1(t) \) for every recorded time step. In Figures 4a and b it is evident that the total current \( i_{tot} \) oscillates according to equation (10) exhibiting a phase angle of approximately 90° with regard to the capacitor voltage \( u_C \). The switching process which transfers \( i_2 \) onto its parallel path is only discernible in \( i_1 \) and \( i_2 \) thus validating the design criterion of non-interference between the current source and the bus-transfer process. Despite the differences in bus-transfer switching time \( t_{BT} \) and thus energy dissipated by the switching arc the frequency \( f_S \) of \( i_{tot} \) is the same in both examples and solely determined by the LC current source. This gives further evidence to negligible feedback from the switching process into the current source. As a result, the power frequency recovery voltage \( u_2^{rv}(t_e) \) appearing between the DS poles immediately after switching is solely determined by the inductive and resistive voltage drop caused by \( i_{tot} \) over the components \( L_1 \) and \( R_1 \) in the parallel path. It is important to note, however, that \( u_2^{rv}(t_e) \) does not contain high-frequency transient recovery voltage (TRV) components due to the differences in surge impedance between the test setup and real substations. If correct representation of TRV is needed, additional components can be added to the test circuit as suggested in IEC 62271-102.

Table 2: Key parameters of the measurements presented in Figure 4.

<table>
<thead>
<tr>
<th>( u_0^C ) [kV]</th>
<th>( i_{tot} ) [kA]</th>
<th>( i_1 ) [kA]</th>
<th>( i_2 ) [kA]</th>
<th>( f_S ) [Hz]</th>
<th>( u_{DS}(t_e) ) [V]</th>
<th>( u_2^{rv}(t_e) ) [V]</th>
<th>( t_{BT} ) [ms]</th>
</tr>
</thead>
<tbody>
<tr>
<td>( a ) 5.0</td>
<td>1.52</td>
<td>0.30</td>
<td>1.27</td>
<td>54.8</td>
<td>-15</td>
<td>0</td>
<td>1.4</td>
</tr>
<tr>
<td>( b ) 5.0</td>
<td>1.51</td>
<td>0.23</td>
<td>1.29</td>
<td>54.8</td>
<td>-18</td>
<td>-17</td>
<td>14.4</td>
</tr>
</tbody>
</table>

The expected distribution of currents prior to the onset of the switching process can be confirmed by comparing the measured maximum values of the currents \( i_1 \), \( i_2 \) and \( i_{tot} \) in the Table 2. It is nonetheless important to note the difference in phase angles between \( i_1 \) and \( i_2 \) in the two examples. Due to the similar power factors of both parallel paths in example \( b \), the currents exhibit only a minimal difference in phase angle. However, due to the comparatively high ohmic resistance in the DS path as compared to the parallel path of example \( a \), a phase difference of 40° is prevalent. Furthermore, the assumption of a constant switching arc voltage \( u_{DS} \) used to find equation (3) can be verified for the type of GIS DS used in these examples. Figures 4c and 4d show a switching arc voltage mostly independent of the switching current \( i_2 \) for short switching times. Despite the reignition after the first current zero in example \( b \), the reappearing arc voltage of opposite polarity again remains approximately constant until the current is brought to zero for a second time. An increase in the arc voltage can be expected due to the increasing distance between the DS electrodes. These results are in good agreement with similar results published by Neumann [6].

To demonstrate the proof of concept’s ability to control individual variables of the bus-transfer process over a considerable magnitude, results from a third example are presented in Figures 5a and b. For this test, path one from example \( b \) was used to represent approximately 550 m of GIS and path two was directly connected to the DS as previously in example \( a \) in order to achieve a more severe condition in terms of preswitching current distribution. Figure 5a shows that prior to the switching process the total current \( i_{tot} \) flows almost entirely through the DS. The initial current was chosen to be 3 kA, almost twice the rated bus-transfer current of the employed DS. As a result of this non-standardized stress, a bus-transfer switching time of 42.6 ms including three reignitions can be seen in Figure 5b. The aforementioned increase in switching arc voltage is evident in said figure from an initial voltage of -20 V to 40 V after the final reignition.
Since the bus-transfer switching process covers more than two periods of the driving current, a significant decrease in magnitude of $i_{tot}$ is apparent. This decrease stems mainly from the power loss at the source resistance $R_S$. For tests with a high demand to current stability it is thus necessary to either increase the energy stored in the capacitors initially or to decrease the ohmic losses in the source.

**CONCLUSION**

The purpose-built impedances are able to accurately model GIS bus over an extensive range of different lengths while also providing a widely adjustable power factor. This combination enables non-standard tests demanding precise control over the parallel impedances such as fault analysis, limit testing or low-frequency applications. The proof of concept LC-resonance current source constructed to provide a finely adjustable AC current in terms of magnitude and frequency has demonstrated the ability to drive a damped sinusoidal current without interaction from the bus-transfer switching process. As a result, the currents through the DS under test represent the conditions found in a grid-connected substation before and during the bus-transfer process with high precision. In addition, the recovery voltage appearing on the poles of the DS after a current zero is determined exclusively by the inductive and resistive voltage drop over the parallel impedances without feedback from the current source. Despite the GIS-specific design of the presented proof of concept test setup, the identical concept can be adapted for other types of switchgear such as AIS and hybrid substations by providing suitable impedances and increased initial energy storage. Thus it can be concluded that the presented bus-transfer test method of using two parallel impedance paths in combination with an LC-resonance current source provides a viable alternative to the traditional method according to IEC 62271-102, particularly for applications where precise and decoupled control over the influencing factors is needed.

**BIBLIOGRAPHY**


